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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,495	08/31/2000	Salman Akram	3847US (98-541)	3659

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EXAMINER
PAREKH, NITIN .

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/652,495	Akram
Examiner	**Art Unit**
Nitin Par kh	2811

-- Th MAILING DATE of this communication appears on th c v r she t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jan 28, 2002

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-72 is/are pending in the applica

4a) Of the above, claim(s) 57-72 is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-56 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US Pat. 6004867) in view of Igarashi et al (US Pat. 5990546), Gaul (US Pat. 5682062) and Gnadinger (US Pat. 5229647).

Regarding claims 1-8, 19, 21, 22, 30-34, 42-44, 50-52 and 56, Kim et al disclose a chip scale package (CSP)/flip chip carrier (FCC) comprising:

- a semiconductor device/silicon chip (110 in Fig. 2) including an active surface, the device being disposed/invertedly disposed adjacent a semiconductor substrate
- the semiconductor substrate (120 in Fig. 2) comprising the same material such as silicon (Col. 3, line 51) having substantially the same coefficient of thermal expansion (TCE) as that of the device/chip, the substrate being disposed adjacent the active

surface and including electrically conductive vias filled with an electrically conductive material (123 in Fig. 2; Col. 4, line 15) and traces in communication with corresponding bond pads (112 in Fig. 2) of the device

- an electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from the substrate opposite to the device and in communication with and being adjacent to respective electrically conductive vias (Fig. 1 and 2; Col. 2, line 62- Col. 4, line 40).

Kim et al fail to disclose:

a) forming the vias through the substrate which extend substantially directly through the substrate and the vias being substantially aligned/in-contact/bonded with corresponding bond pads of the device, and

b) substantially laterally extending conductive trace in communication with the via.

a) However, Kim et al disclose forming traces (122 in Fig. 2) using conventional patterning/wafer scale processing such that the pads and vias (124/123 in Fig. 2) can be formed at any desired position on the surface of the substrate with respect to the position of the device pads (112 in Fig. 2; Col. 4, line 9-25).

Kim et al further disclose forming direct vertical connections between vertically separated trace/metal layers using conventional through-holes (Col. 4, line 55).

Igarashi et al teach using a CSP/FCC conventional vias (212a in Fig. 4) through the wiring plate/substrate which extend substantially directly through the substrate and substantially align with corresponding bond pads (11a in Fig. 4) of the device (1 in Fig. 4; Col. 6, line 40- Col. 7, line 7).

b) Gaul teaches using vertically aligned vias through the silicon substrates (320a, 320b, etc. in Fig. 4P and 4J-N) which extend substantially directly through the substrates and the vias further comprising a variety of substantially laterally extending conductive trace/metallization layers (336 in Fig. 4P, 331 in Fig. 4N, 444 in Fig. 4D, etc.) in communication with respective electrically conductive vias to provide direct vertical connection between the silicon substrates (Col. (Col. 9, line 45- Col. 10, line 60).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate vias comprising the elements a) and b) to improve the bonding strength and reliability of via/bump interconnection using Igarashi et al and Gaul's through-hole design in Kim et al's package.

Regarding claims 9, 10, 35 and 36, Kim et al disclose a first thickness of the semiconductor device/chip (110 in Fig. 2) being greater than that of the semiconductor substrate (120 in Fig. 2) but fail to specify those being substantially the same.

It is a matter of design choice in CSP fabrication and wafer level packaging to select parameters such as a thickness/area/shape of the substrates, diameter/height/spacing of solder balls, via dimensions, etc. to achieve the desired package size, rigidity and interconnection density requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device and the substrate having substantially the same thickness to achieve the desired package size, weight and rigidity in Kim et al's package in view of Igarashi et al and Gaul .

Regarding claims 11-14, 37-41 and 45-49 Kim et al disclose forming conventional metallization layers comprising pads, traces, etc. on the top and bottom surfaces of the substrate but fail to show a reference numeral in Fig. 1-3 for an insulating material substantially extending over the substrate surface opposite to the device.

However, Kim et al further disclose using conventional wafer level fabrication including deposition and patterning processes where the pads and traces are formed in the device/substrate being exposed through the insulating/passivating layers (114, 214,

314, etc. in Fig. 2-5B) such as a silicon oxide, nitride, etc extending over the substrate surface (Col. 3, line 1; Col. 4, line 16- Col. 5, line 64).

Gnadinger teaches using conventional wafer level fabrication including via and bump formation processes where an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc extends over the substrate surface opposite to that of the device pad and the via being exposed through the insulating material (Col. 4, line 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an insulating material comprising silicon oxide substantially extending over the substrate surface opposite to the device to achieve the desired insulation and surface protection using Gnadinger, Igarashi et al and Gaul's teachings in Kim et al's package.

Regarding claims 15-18, 26-29 and 53-55 as explained above for claims 11-14, Kim et al in view of Igarashi et al and Gaul disclose using the electrically conductive vias and corresponding bond pads in communication through the intermediate passivation layer but fail to specify using the intermediate layer an adhesive material or polyimide.

It is conventional in CSP fabrication and wafer level packaging art to use passivation/dielectric layers such as polyinimde, adhesive/resin, etc. between the chip and the substrate to provide improved surface protection and insulation. Igarashi et al

teach using a conventional sealing resin/adhesive (3 in Fig. 3I and 4; Col. 6 and 7) in the intermediate layer between the device and wiring plate/substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising an adhesive material or polyimide to achieve the desired insulation and surface protection in Kim et al's package in view of Igarashi et al and Gaul.

Regarding claims 20 and 23-25, as explained above, Kim et al discloses a region comprising bond pad, via and respective material but fail to specify forming a diffusion region securing the device to the substrate.

However, as explained above for claims 1 and 19, Kim et al disclose using conventional high temperature/thermo-compression processing in the range of 300-100 deg. C to provide an electrical and mechanical bonding of the bond/terminal pads, traces, conductive vias, etc. of the device and substrate (Col. 3, line 47; Col. 5, line 47).

Gnadinger teaches using a wafer scale package where a diffusion region is formed comprising via, bond pad and respective material (23 in Fig. 4; Col. 4, line 23)

It would be obvious to one of ordinary skill in the art at the time invention was made to realize that a diffusion region between the bond pad and via and comprising the respective material would be formed securing the device to the substrate in Kim et al's package in view of Gnadinger, Igarashi et al and Gaul.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

04-02-02

Steven Loke